

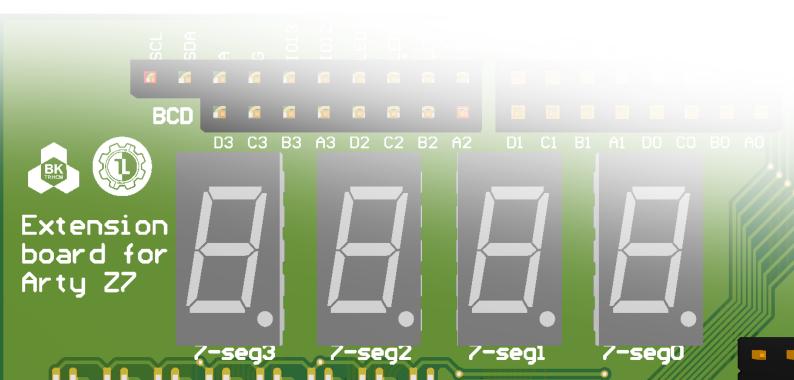
#### User Manual

## Extension board for Arty Z7

Ho Chi Minh City, 2023

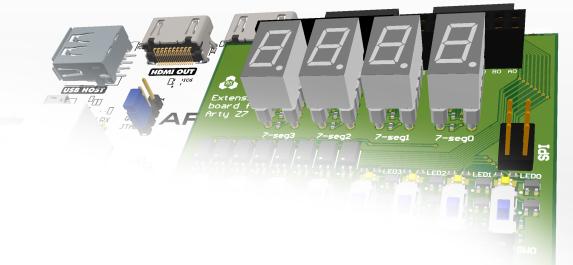
#### **Features**

- 8 extended switches
- 4 extended single LEDs
- 4 extended seven-segment LEDs



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## Part I

# Introduction to Extension board for Arty Z7

## Extension board for Arty Z7

#### 1.1 Overview

Extension board for Arty Z7 is used for FPGA Arty Z7 board, extended more switches, single LEDs, and seven-segment LEDs. The Extension board is used to support for Logical Design with verilog HDL subject, helps students use the extended functions that the Extension board supports. All functions are connected through the headers used to connect the Arty Z7 and other peripherals.

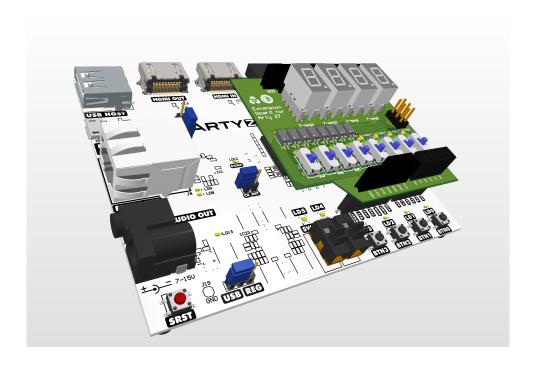


Figure 1.1: Extension board for Arty Z7



#### 1.2 Package contents

Extension board for Arty Z7 package includes:

- The Extension board.
- $\bullet$  Constraint file "Arty-Z7-20-Extension-board-Master.xdc".

#### 1.3 Getting helps

Here are the address where you can get help if you encounter any problems:

- Fanpage: https://www.facebook.com/thiennhan.hardware/
- Email: thiennhan.hardware@gmail.com

# Extension board's Layout

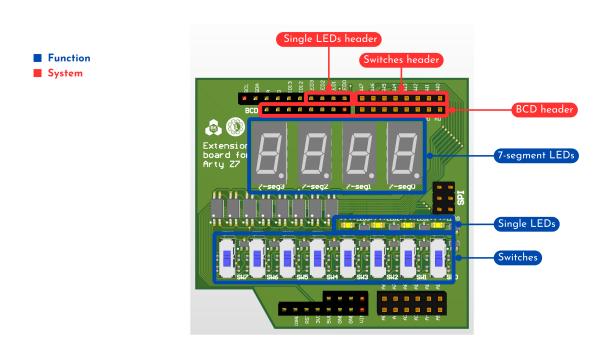


Figure 2.1: Extension board's layout

# Getting Started

#### Attention

Before Arty Z7 is powered, or uploaded code, all the switches must be set at the LOW level and the pins connected to the Arty Z7 must be configured as LVCMOS33 standard.

#### Connecting the Extension board onto Arty Z7

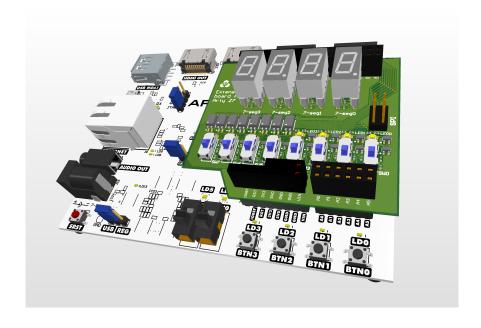
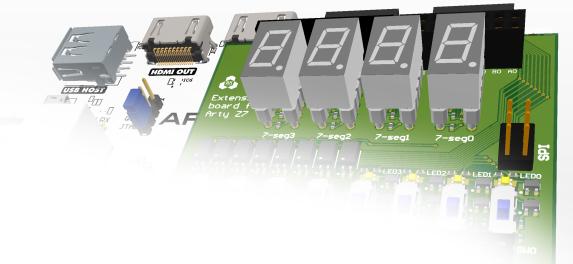


Figure 3.1: The Arty Z7 with connected Extension board



## Part II

# Extension board for Arty Z7 GUIDELINE

# Pin Configurations on Arty Z7

| PIN TYPE | PACKAGE PIN | FUNCTION      |
|----------|-------------|---------------|
| Switches |             |               |
| SW0      | T14         | Digital input |
| SW1      | U12         | Digital input |
| SW2      | U13         | Digital input |
| SW3      | V13         | Digital input |
| SW4      | V15         | Digital input |
| SW5      | T15         | Digital input |
| SW6      | R16         | Digital input |
| SW7      | U17         | Digital input |

| PIN TYPE    | PACKAGE PIN | FUNCTION             |
|-------------|-------------|----------------------|
| Single LEDs |             |                      |
| LED0        | V17         | Digital input/output |
| LED1        | V18         | Digital input/output |
| LED2        | T16         | Digital input/output |
| LED3        | R17         | Digital input/output |



| PIN TYPE                    | PACKAGE PIN | FUNCTION                      |  |  |
|-----------------------------|-------------|-------------------------------|--|--|
| Seven-segment LEDs          |             |                               |  |  |
| $7\text{-seg}0\_A$          | U5          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}0\_B$          | V5          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}0\_\mathrm{C}$ | V6          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}0\_D$          | U7          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg1}_A$           | V7          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg1}_{B}$         | U8          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg1}_{\text{C}}$  | V8          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg1}_D$           | V10         | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}2\_A$          | W10         | Digital input/output          |  |  |
| $7\text{-seg}2\_B$          | W6          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}2\_C$          | Y6          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}2\_D$          | Y7          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}3\_A$          | W8          | Digital input/output          |  |  |
| $7\text{-seg}3\_B$          | Y8          | ${\bf Digital\ input/output}$ |  |  |
| $7\text{-seg}3\_C$          | W9          | ${\bf Digital\ input/output}$ |  |  |
| 7-seg3_D                    | Y9          | Digital input/output          |  |  |

## Functions on Extension board

#### 5.1 Switches

There are 8 switches used to generate logic level for Arty Z7 or other peripherals. These switches must be configured as digital input (detailed instruction provided in Chapter 6), otherwise, it may damage Arty Z7.

When a switch is pulled up, the corresponding header pin will generate a HIGH logic level and its green LED will turn on. Contrarily, a pulled-down switch indicates a LOW logic level in the corresponding pin and its green LED will turn off.

To use switches, please configure the corresponded pins be digital input. The switches create logic level into Arty Z7 or connected peripherals.

Note: Please don't configure output pin for switches, it may damage Arty Z7.

#### 5.2 Single LEDs

The Extension board supports 4 single LEDs. The LED will be on at HIGH logic level and will be off at LOW logic level.

The pins used to control single LEDs must be configured as follows:

- When Arty Z7 generate signal to control the LEDs, the corresponding pins must be configured as digital output. Signal from that pin can also be used by peripherals.
- When peripherals generate signal to control the LEDs, the corresponding pins must be configured as digital input. Signal from that pin can also be used by Arty Z7.



#### 5.3 Seven-segment LEDs

The Extension board supports 4 seven-segment LEDs that is controlled by BCD code. The LEDs only display the number from 0 to 9, the rest will be blank.

*Note:* The dot segment is disable.

To use seven-segment LEDs, the user may configure the corresponded pins be digital input or output similar to how the pins are configured in the single LEDs section above.

# Setting I/O Ports on Vivado

The user write code verilog using the function on the Extension board.

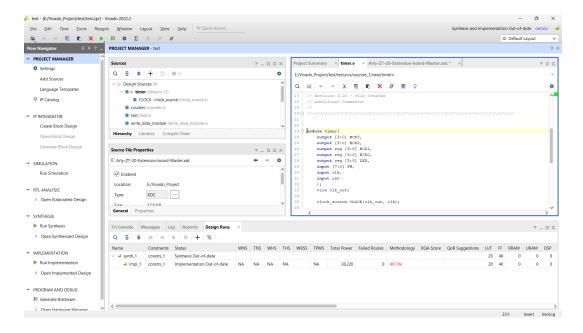


Figure 6.1: Verilog code



The user's constraint file used to configure pins must be selected "Set as Target Constraint File".

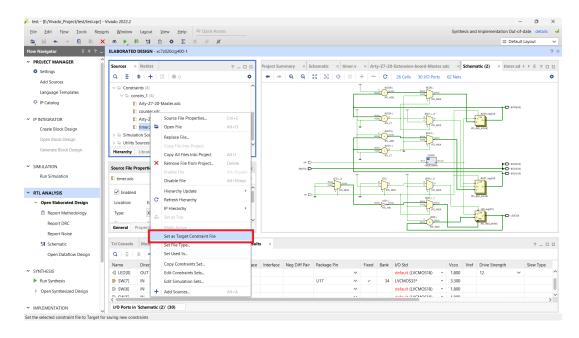


Figure 6.2: Set as Target Constraint File

Open Schematic  $\rightarrow$  I/O Ports, and on the screen will display the table to configure I/O Ports.

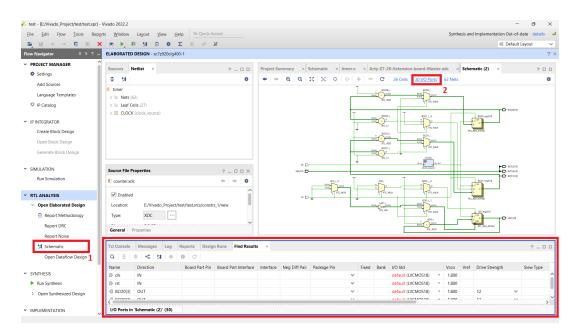


Figure 6.3: I/O Ports



The Package Pin and I/O Std for corresponded pin must be configured based on constraint file "Arty-Z7-20-Extension-board-Master.xdc". For example, to set input pin SW[7] be switch SW7 on Extension board, Package Pin is configured to U17 and I/O Std is configured to LVCMOS33.

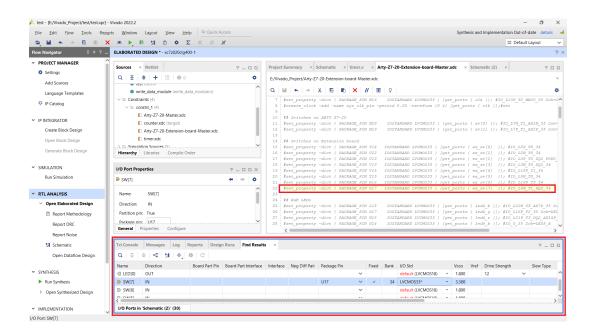


Figure 6.4: I/O Ports setting

After save the setting, constraint file created previously will auto-setup for I/O pins in Generate Bitstream process.

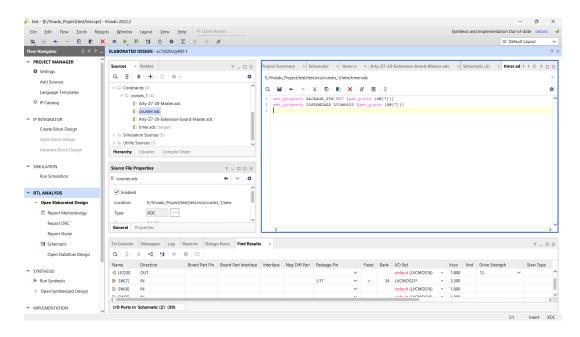
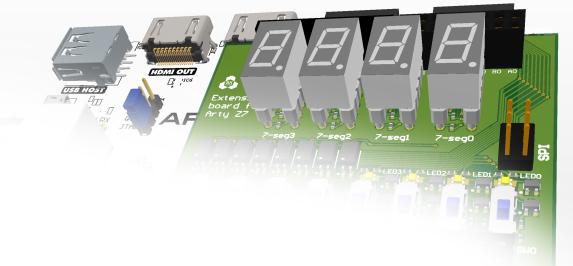


Figure 6.5: Constraint file



# Part III

# Appendix

# Revision History

| Version | Change Log      |
|---------|-----------------|
| V1.0    | Initial Version |